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BEFORE THE BOARD OF PATENT APPEALS AND INTERFERENCES

Application Number: 10/665,906
Filing Date: September 18, 2003
Appellant(s): RAO, G.R. MOHAN

Robert A. Voigt Jr.
For Appellant

EXAMINER'S ANSWER

This is in response to the appeal brief filed December 6, 2006 appealing from the Office action mailed October 20, 2006.

(1) Real Party in Interest

A statement identifying by name the real party in interest is contained in the brief.

(2) Related Appeals and Interferences

The examiner is not aware of any related appeals, interferences, or judicial proceedings which will directly affect or be directly affected by or have a bearing on the Board's decision in the pending appeal.

(3) Status of Claims

The statement of the status of claims contained in the brief is correct.

(4) Status of Amendments After Final

The appellant's statement of the status of amendments after final rejection contained in the brief is correct. Examiner notes that although there have been no after final amendments submitted after the final rejection of July 26, 2006, there has been an amendment after the subsequent non-final rejection of October 20, 2006, filed with the appeal brief of December 6, 2006.

(5) Summary of Claimed Subject Matter

The summary of claimed subject matter contained in the brief is correct.

(6) Grounds of Rejection to be Reviewed on Appeal

The appellant's statement of the grounds of rejection to be reviewed on appeal is correct. Examiner notes that after further review, all rejections over Curtis et al., US 6,925,086 B2 are hereby withdrawn.

(7) Claims Appendix

The copy of the appealed claims contained in the Appendix to the brief is correct.

(8) Evidence Relied Upon

5,440,523	JOFFE	8-1995
6,424,658 B1	MATHUR	7-2002

Microsoft Press, "Computer Dictionary", Second Edition, 1994, p. 418.

(9) Grounds of Rejection

The following ground(s) of rejection are applicable to the appealed claims:

Claims 1-21 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention. Appellant has argued that Joffe and Mathur do not disclose an array as recited in claims 1, 8, and 16, stating that the limitation "single column of predetermined word-width" must be read consistent with the interpretation those of skill in the art would reach.

First, the limitation of a single column is apparently a single vertical arrangement of elements. It is a trivial matter that such a vertical arrangement may be considered combined with a similar, adjacent vertical arrangement into a single, wider vertical arrangement. For example, Appellant's own invention includes a vertical arrangement of a plurality of 384 bit wide elements one on top of the other, and thus as two examples might be considered as a single column, or 384 adjacent one bit-wide columns. The columns of any references likewise may be considered combined as desired since combining columns in any manner also results in a column. Any argument against this must be based on a "single column" having some structure or function that is not met by a combination of two or more adjacent columns. No such structure or function is

claimed, disclosed, or argued. Thus, if the argument that the references do not have a single column of predetermined word-width is based on the limitation "single column", it is not apparent what the limitation "single column" is intended to cover, if not simply a vertical arrangement of elements.

Second, the terms "word" and "word-width" (synonymous with "word length") are well defined in the art. According to Microsoft Press Computer Dictionary, word length is the largest amount of data handled by a microprocessor in one operation, or the width of the main data bus, typically 8, 16, or 32 bits. Appellant's meaning for word-width includes the particular example of a width of 384 bits. This is apparently beyond the normal meaning of the term (Examiner is not aware of any microprocessor that operates on 384 bits in one operation). Therefore it is contended that one of skill in the art would interpret the term "word-width", consistent with the specification, to comprise simply a length of data that is handled in one operation, and may include transfer on a bus of that width. The rows of the references are transferred and handled in one operation. Thus, if the argument that the references do not have a single column of predetermined word-width is based on the limitation "predetermined word-width", it is not apparent what the limitation "predetermined word-width" is intended to cover, if not a length of data that is handled in one operation.

Claims 2-7, 9-15, and 17-21 incorporate these limitations by dependency.

Claims 1-2, 7, 16-17 are rejected under 35 U.S.C. 102(b) as being anticipated by Joffe, US 5,440,523.

As to claims 1-2 and 16-17, Joffe discloses a *switch/system comprising ports for exchanging data between resources, and shared memory* (see Abstract, Figs. 1 and 2, col. 1 lines 13-19) *comprising an array of cells arranged as rows and a single column having a width equal to a predetermined word width* (Figs. 1 and 2, the shared memory having a single column having a word width of k x m bits, see col. 2 lines 7-29, in particular "all k-words of the burst are simultaneously transferred from the buffer and written to the shared memory on the k x m path", and thus what Joffe calls a word, the m-bit wide words transferred between the ports and the Memory Access Buffers, are combined in the buffers and transferred in a single operation as a k x m bit wide transfer to a fill a single row of the shared memory, this k x m bit wide transfer reading on the claimed word-width), *circuitry for writing selected data at a port to a selected row as a word of the word width during a first time period, and read it during a second time period for output at a second port* (see col. 1 lines 53-64 and col. 2 lines 30-49); *converts from initial bit-width to predetermined width* (k to k x m).

As to claim 7, the array of Joffe is as a random access array of read/write classification (see Joffe claim 1).

Claims 1-3, 5-8, 10-17, and 20 are rejected under 35 U.S.C. 102(b) as being anticipated by Mathur, US 6,424,658 B1.

As to claims 1, 7, 16, and 20, Mathur discloses a *switch/system comprising ports for exchanging data* (see Abstract, Fig. 2), and *shared RAM memory comprising an array of cells arranged as rows and a single column having a width equal to a predetermined word width* (See Figs. 2 and 3, memory 20 having a single column since

a column can be defined as having the width of the longest entry for a single packet, such as packets 3 and 6 in Fig. 9, where the claimed predetermined word-width is equal to the length of those longest packets, see col. 4 lines 31-34 "writes an entire packet to a row of the embedded packet memory without interruption", considered as one operation and thus a word-width as recited. Alternatively, memory 20 has a single column such as col. 1 in Fig. 9, where the claimed memory array may be considered only that column of the array of Mathur, since the entire memory structure does not need to be considered to read on the claim language, further, the predetermined word-width is considered the 256 bit width of col. 1, which is transferred in one operation across the 256 bit wide data bus 42, Fig. 3, see col. 11 lines 25-36, and thus a word-width as recited), *circuitry for writing selected data at a port to a selected row as a word of the word width during a first time period, and read it during a second time period for output at a second port* (see Figs. 6 and 7, also in general col. 1 line 55 to col. 2 line 11, col. 4 lines 31-44, col. 5 lines 56-61, which states that column address is not required, supporting the assertion that the memory may be thought of as a single column, also col. 11 lines 44-56).

As to claims 2 and 17, Mathur discloses buffers converting the bit-widths (see col. 6 lines 36-65).

As to claim 3, in Mathur each packet inherently contains certain bit width and associated overhead.

As to claims 5-6, Mathur discloses available and used address tables (tables 60 and 80 respectively, one each for each port, see Figs. 6 and 7, see col. 9 lines 8-25, and col. 10 lines 1-15).

As to claims 8 and 11-15, Mathur discloses the invention substantially as described above with regard to claims 1-7. Mathur additionally discloses a buffer at each port assembling the data stream as recited (see col. 6 lines 36-65). Memory 20 may be considered a plurality of banks (as vertically divided for ports as shown in Fig. 9).

As to claim 10, the input port table in Mathur operates as a FIFO as recited.

Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Joffe, US 5,440,523.

As to claim 3, the embodiment of Joffe cited with regard to claims 1-2 hereinabove (Figs. 1 and 2) does not disclose the bit width includes data and associated overhead. However, another embodiment (Fig. 3) discloses data along with parity (see col. 2 lines 52-57). Parity is one type of overhead associated with data. It would have been desirable to include the parity in the first embodiment, because it is a well known means of preserving data integrity. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to include data and associated overhead, because it was taught by Joffe in a similar embodiment, and is one type of overhead which was known to preserve data integrity.

As to claim 4, the system of Joffe has the inherent capability of having bit widths of 48 and 384 as recited (by way of the k and the k x m bit widths).

Claims 4, 9, 18-19, and 21 are rejected under 35 U.S.C. 103(a) as being unpatentable over Mathur.

As to claims 4, 9, Mathur does not disclose initial bit width 48 or predetermined bit width of 384. As to claims 18-19, Mathur does not disclose ATM format. As to claim 21, Mathur does not disclose the recited data interfaces. Each of these limitations were obvious and well known at the time of the invention. The specific bit widths recited fall within the envisioned embodiments of a clearly scalable bit size. Advantages of using ATM format were notoriously well known (such as compatibility with others using the format). Interfaces such as DDR were widely known to have performance benefits. Strobing on both clock edges is akin to DDR and was known to improve performance. Thus it would have been obvious to one of ordinary skill in the art at the time of the invention to add any of these elements, because they and their advantages as stated above were widely known at the time.

(10) Response to Argument

Appellant's response to the 35 USC 112 second paragraph rejection (pages 4-7 of the brief) simply cites the specification, but the cited sections do not clarify these limitations of the claims (in light of related assertions by Appellant that the references doe not disclose them), and so the rejection is maintained hereinabove. That is, it is not apparent why two identical adjacent columns may not be considered as combined into a single column, absent any further defining characteristics of a "single column" other than a vertical arrangement of elements. Also, it is not apparent that when rows of the references are transferred in a single operation, why those rows might not be properly

considered of a "predetermined word-width", absent any further defining characteristics of a "predetermined word-width" other than a data length handled in a single operation. It is noted that the statement on page 7 of the brief that the Examiner admitted the limitation in claims 4 and 9 is novel is incorrect; it was admitted that a microprocessor handling a data width of 384 bits in one operation was not known to the Examiner, but claims 4 and 9 only require a word-width of 384 bits in accordance with Appellants disclosure of what a word-width is (apparently, a data length handled in one operation, not necessarily in the registers of a microprocessor).

Appelllants have argued (pages 7-9 of the brief) that Joffe does not disclose a memory arranged as a single column of predetermined word-width. Examiner disagrees. As cited hereinabove "all k-words of the burst are simultaneously transferred from the buffer and written to the shared memory on the k x m path", so the k x m data length, which is transferred in one operation, may be properly considered a word width as disclosed by Appellant. Since this width takes up an entire row of a given row of the shared memory of Joffe, that memory may be considered a single column of that width. Appellant makes further arguments that Joffe does not disclose writing selected data present at a port to a selected row during a first time period, and reading it during a second time period. Examiner disagrees. That is exactly what Joffe does; whether or not there is any preselection of data or rows, data that is transferred as cited in Joffe must be selected and the row to which it is written must be selected. Appellants have argued that Joffe does not disclose a digital switch coupling resources exchanging data in a selected digital format. All data is exchanged in a selected digital format (such as

binary, etc.), and the purpose of the multiple port shared memory of Joffe is to allow resources to exchange data, and thus composes a digital switch as recited (see col. 1 lines 6-19).

Appellants have argued (pages 10-11 of the brief) that Joffe does not convert an initial bit-width to the predetermined bit-width. Examiner disagrees. That is exactly what Joffe does; the bit-width of m is converted to the bit-width of k x m as shown in Figs. 1 and 2 of Joffe. Appellants have argued that Joffe does not disclose a random access array. Examiner disagrees; the memory is disclosed as RAM in the claims (see claim 1 line 2), and any RAM is read/write as recited. Appellants have argued that Joffe does not exchange data through the ports as streams of words of initial word-width. Examiner disagrees; Joffe shows in Figs. 1 and 2, and in the cited sections an I/O port burst of m-bit width words, and burst being a continuous stream of words.

Appellants have argued (pages 12-14 of the brief) that Examiner must provide evidence that columns 1-48 of Mathur may be interpreted as a single column of predetermined word-width. However, as described in the 35 USC 112 rejection above, Appellant has not defined a "column" with enough specificity to prevent its reading on multiple columns of Mathur. Since a column is simply a series of elements arranged vertically, it is trivial that a plurality of columns may be considered a single column; there is no claimed limitation on how wide a column may be, other than a word-width wide. It is also maintained that, consistent with the specification, the transfer of a packet to an entire memory row in Mathur may be seen as a predetermined word-width, since it is handled as a unit and transferred in a single operation.

Appellants have argued (pages 14-16 of the brief) that Mathur does not teach circuitry for writing as recited; Examiner disagrees since all word widths as interpreted above are written and read (see Mathur col. 3 line 66 to col. 4 line 2), clearly during different time periods to the extent recited. Appellants have argued (pages 16-17 of the brief) that Mathur does not teach a buffer associated with each port assembling a data stream as recited; Examiner disagrees, the packet buffers are used to assemble a data stream input into packets and vice versa, and are associated with each port as shown in Fig. 3, as recited. A buffer in each port is associated with that port. Alternatively, the claimed port may be considered all elements of the port of Mathur except for the buffer. Appellants have argued that Mathur does not teach shared memory effecting a transfer from one to another port through corresponding buffers, however, all transfers to and from the switch are made through port buffers using the shared memory.

Appellants have argued (pages 17-19 of the brief) that Mathur does not teach banks. As previously argued by the Examiner, the banks may be considered to be the vertically portioned sections of Fig. 9, such as PORT A, and PORT C; "bank" in general is simply some section or partition of memory, and Appellants have provided no argument that it should be considered otherwise. See Mathur col. 11 lines 37-38, "the packet memory is divided into several regions, one for each input port". Appellants have argued (pages 19-20 of the brief) that Mathur does not teach the plurality of address tables for writing and reading as recited. Examiner disagrees. Figs. 6 and 7 show representative tables maintaining addresses for Port A, Fig. 6 controlling those that may be written (available), Fig. 7 controlling those that may be read (used), and at

least the counters of those figures count to the end of a packet and thus output from the table as a queue.

Appellants have argued (page 21 of the brief) that Mathur does not convert from an initial bit width to a predetermined bit width. Examiner disagrees; the bit conversion is disclosed at col. 6 lines 31-40 and in Fig. 6. Appellants have argued (page 22 of the brief) that Mathur does not teach bit-width and overhead, but Examiner maintains that it is well known that the packets as described therein contain data plus overhead. Contrary to Appellant's assertions, one skilled in the art would have known those packets to contain both data and overhead. Appellants have argued (page 23 of the brief) that Mathur does not teach address table operating as FIFO, but at least the counters of Fig. 6 and 7 operate by counting to the end of a packet, thus outputting from the table as a queue, which is the same as a FIFO operation. Appellants have argued (page 24 of the brief) that limitations of claims 11-15 have not been shown; Examiner disagrees since the memory is a DRAM, stores data corresponding to port, and may include any desired number of ports (that may be more than the number of banks). Appellants have argued (page 25 of the brief) that the limitation of selection from types of resources has not been shown; Examiner disagrees since Mathur has selected a network switch, and thus at least for a digital data network.

Appellants have argued (pages 31-32 of the brief) that parity is not overhead. Since parity is an extra bit or bits that are generated from existing data to provide for error protection, it is in fact overhead as recited. Appellants have argued that Joffe

does not teach bit-widths of 48 and 384 bits. Since Joffe uses variables m and k x m for these widths respectively, any possible width is contemplated.

Appellants have argued (pages 32-37 of the brief) that Examiner has not provided the motivation required to modify the references as stated in the 35 USC 103 rejection; Examiner disagrees since the limitations in question were either within known scaleable variations (different bit widths for a reference that recognizes that different bit widths may be desired by designating them variable), or widely known and providing performance benefits as stated hereinabove (ATM, DDR, strobing).

(11) Related Proceeding(s) Appendix

No decision rendered by a court or the Board is identified by the examiner in the Related Appeals and Interferences section of this examiner's answer.

For the above reasons, it is believed that the rejections should be sustained.

Respectfully submitted,

Gary J. Portka

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